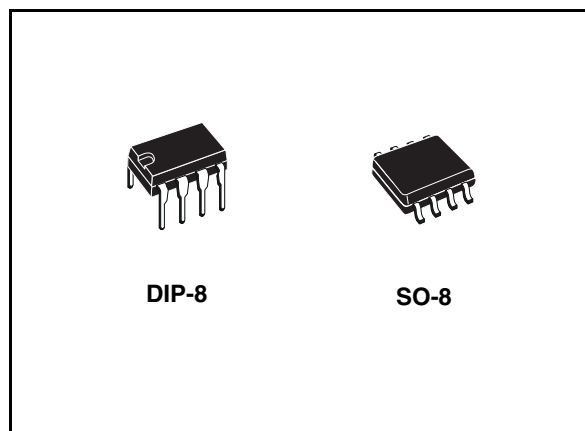


3.3 V powered, 15 kV ESD protected,
up to 12 Mbps true RS-485/RS-422 transceiver

Features

- ESD protection
 - ± 15 kV human body model
 - ± 8 kV IEC 1000-4-2 contact discharge
- Operate from a single 3.3 V supply - no charge pump required
- Interoperable with 5 V logic
- 1 μ A low current shutdown mode max
- Guaranteed 12 Mbps data rate
- -7 to 12 common mode input voltage range
- Half duplex versions available
- Industry standard 75176 pinout
- Current limiting and thermal shutdown for driver overload protection
- Guaranteed high receiver output state for floating, shorted or terminated inputs with no signal present
- Allow up to 64 transceivers on the bus



thermal shutdown circuitry that places the driver outputs into a high-impedance state.

The ST1480A input has a true fail-safe feature that guarantees a logic high output if both inputs are open circuit, shorted together or in the presence of a termination with no signal on the bus.

Description

The ST1480A is ± 15 kV ESD protected, 3.3 V low power transceiver for RS-485 and RS-422 communications. The device contains one driver and one receiver in half duplex configuration.

The ST1480A transmits and receives at a guaranteed data rate of at least 12 Mbps.

All transmitter outputs and receiver inputs are protected to ± 15 kV using Human Body Model.

Driver is short-circuit current limited and is protected against excessive power dissipation by

Figure 1. Device summary

Part number	Temperature range	Package	Packaging
ST1480ACN	0 to 70 °C	DIP-8	50 parts per tube / 40 tube per box
ST1480ACDR	0 to 70 °C	SO-8 (tape & reel)	2500 parts per reel
ST1480ABDR	-40 to 85 °C	SO-8 (tape & reel)	2500 parts per reel

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1 Pin configuration

Figure 2. Pin connections

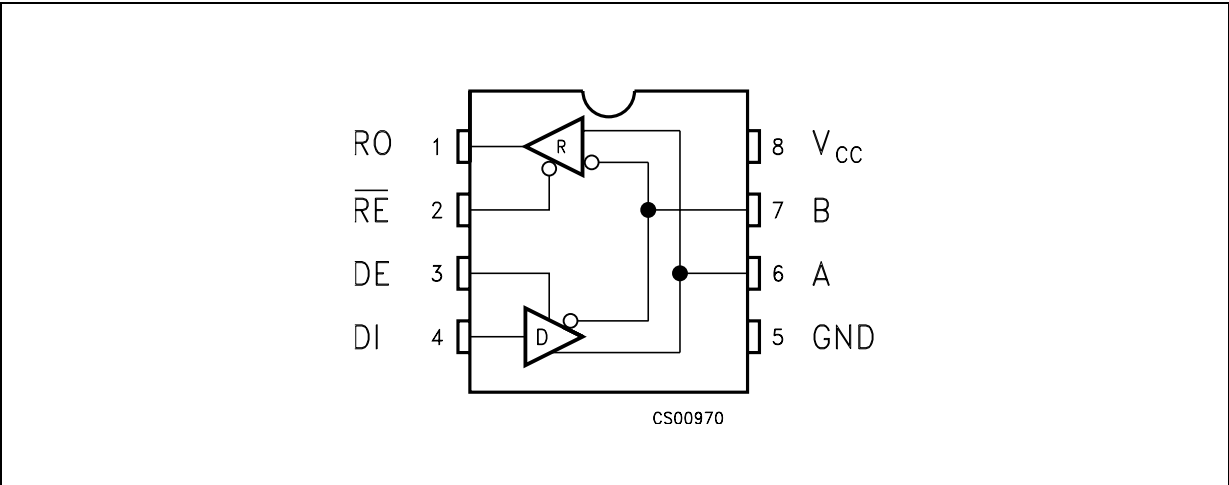


Table 1. Pin description

Pin n°	Symbol	Name and function
1	RO	Receiver output. If A>B by 200mV, RO will be high; if A<B by 200mV, RO will be low
2	$\overline{RE}$	Receiver Output Enable. RO is enabled when RE is low; RO is high impedance when RE is high. If RE is high and DE is low, the device will enter a low power shutdown mode.
3	DE	Driver Output Enable. The driver outputs are enabled by bringing DE high. They are high impedance when DE is low. If RE is high DE is low, the device will enter a low-power shutdown mode. If the driver outputs are enabled, the part functions as line driver, while they are high impedance, it functions as line receivers if RE is low.
4	DI	Driver input. A low on DI forces output A low and output B high. Similarly, a high on DI forces output A high and output B low
5	GND	Ground
6	A	Non-inverting receiver input and non-inverting driver output
7	B	Inverting receiver input and inverting driver output
8	V _{CC}	Supply voltage: V _{CC} = 3V to 3.6V

2 Truth tables

Table 2. Truth table (driver)

Inputs			Outputs		Mode
RE	DE	DI	B	A	
X	H	H	L	H	Normal
X	H	L	H	L	Normal
L	L	X	Z	Z	Normal
H	L	X	Z	Z	Shutdown

Note: X= Don't care; Z=High impedance

Table 3. Truth table (receiver)

Inputs			Output	Mode
RE	DE	A-B	RO	
L	L	$\geq -0.015V$	H	Normal
L	L	$\leq -0.2V$	L	Normal
L	L	Inputs open	H	Normal
L	L	Inputs shorted	H	Normal
H	L	X	Z	Shutdown

Note: X= Don't care; Z=High impedance

3 Maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	7	V
V_I	Control input voltage ($\overline{RE}$, DE)	-0.3 to 7	V
V_{DI}	Driver input voltage (DI)	-0.3 to 7	V
V_{DO}	Driver output voltage (A, B)	± 14	V
V_{RI}	Receiver input voltage (A, B)	± 14	V
V_{RO}	Receiver output voltage (RO)	-0.3 to ($V_{CC} + 0.3$)	V

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 5. ESD performance: transmitter outputs, receiver inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ESD	ESD protection voltage	Human body model		± 15		kV
ESD	ESD protection voltage	IEC-1000-4-2 Contact discharge		± 8		kV

4 Electrical characteristics

Table 6. Electrical characteristics

$V_{CC} = 3\text{ V to }3.6\text{ V}$, $T_A = -40\text{ to }85\text{ }^{\circ}\text{C}$, unless otherwise specified. Typical values are referred to $T_A = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I _{SUPPLY}	V _{CC} Power supply current	No Load, DI=0V or V _{CC}	DE=V _{CC} , RE=0V or V _{CC}		1.3	2.2	mA
			DE=0V, RE=0V		1.2	1.9	mA
I _{SHDN}	Shutdown supply current	DE=0V, RE=V _{CC} , DI=0V or V _{CC}			0.002	1	μA

Table 7. Logic input electrical characteristics

$V_{CC} = 3\text{ V to }3.6\text{ V}$, $T_A = -40\text{ to }85\text{ }^{\circ}\text{C}$, unless otherwise specified. Typical values are referred to $T_A = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input logic threshold low	DE, DI, RE		1.3	0.8	V
V_{IH}	Input logic threshold high	DE, DI, RE	2			V
I_{IN1}	Logic input current	DE, DI, RE			± 2.0	μA
I_{IN2}	Input current (A, B)	DE=0V, $V_{CC} = 0\text{ or }3.6\text{ V}$	$V_{IN}=12\text{ V}$		1	mA
			$V_{IN}=-7\text{ V}$		-0.8	mA

Table 8. Transmitter electrical characteristics

$V_{CC} = 3\text{ V to }3.6\text{ V}$, $T_A = -40\text{ to }85\text{ }^{\circ}\text{C}$, unless otherwise specified. Typical values are referred to $T_A = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OD}	Differential drive output	$R_L = 100\Omega$ (RS-422) (Figure 2)	2			V
		$R_L = 54\Omega$ (RS-485) (Figure 2)	1.5			V
		$R_L = 60\Omega$ (RS-485) (Figure 3)	1.5			V
ΔV_{OD}	Change in magnitude of driver differential output voltage for complementary output states (Note: 1)	$R_L = 54\Omega$ or 100Ω (Figure 2)			0.2	V
V_{OC}	Driver common mode output voltage	$R_L = 54\Omega$ or 100Ω (Figure 2)			3	V
ΔV_{OC}	Change in magnitude of driver common mode output voltage (Note: 1)	$R_L = 54\Omega$ or 100Ω (Figure 2)			0.2	V
I_{OSD}	Driver short circuit output current				± 250	mA

Table 9. Receiver electrical characteristics

$V_{CC} = 3V$ to $3.6V$, $T_A = -40$ to $85^\circ C$, unless otherwise specified. Typical values are referred to $T_A = 25^\circ C$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{TH}	Receiver differential threshold voltage	$V_{CM} = -7V$ to $12V$, $DE = 0$	-0.2		-0.015	V
ΔV_{TH}	Receiver input hysteresis	$V_{CM} = 0V$		30		V
V_{OH}	Receiver output high voltage	$I_{OUT} = -4mA$, $V_{ID} = 200mV$, (Figure 9)	2			V
V_{OL}	Receiver output low voltage	$I_{OUT} = 4mA$, $V_{ID} = -200mV$, (Figure 4)			0.4	V
I_{OZR}	3-State (high impedance) output current at receiver	$V_{CC} = 3.6V$, $V_O = 0V$ to V_{CC}			± 1	μA
R_{RIN}	Receiver input resistance	$V_{CM} = -7V$ to $12V$	24			k Ω
I_{OSR}	Receiver short-circuit current	$V_{RO} = 0V$ to V_{CC}	7		60	mA

Table 10. Driver switching characteristics

$V_{CC} = 3V$ to $3.6V$, $T_A = -40$ to $85^\circ C$, unless otherwise specified. Typical values are referred to $T_A = 25^\circ C$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
D_R	Maximum data rate		12	15		Mbps
t_{DD}	Differential output delay	$R_L = 60\Omega$, $C_L = 15pF$, (Figure 5 and Figure 6)		18	30	ns
t_{TD}	Differential output transition time	$R_L = 60\Omega$, $C_L = 15pF$, (Figure 5 and Figure 6)		12	20	ns
t_{PLH} t_{PHL}	Propagation delay	$R_L = 27\Omega$, $C_L = 15pF$, (Figure 9 and Figure 10)		18	30	ns
t_{PDS}	$ t_{PLH} - t_{PHL} $ propagation delay skew (Note 2)	$R_L = 27\Omega$, $C_L = 15pF$, (Figure 9 and Figure 10)		2	5	ns
t_{PZL}	Output enable time	$R_L = 110\Omega$, (Figure 11 and Figure 12)		19	35	ns
t_{PZH}	Output enable time	$R_L = 110\Omega$, (Figure 7 and Figure 8)		30	50	ns
t_{PHZ}	Output disable time	$R_L = 110\Omega$, (Figure 7 and Figure 8)		19	35	ns
t_{PLZ}	Output disable time	$R_L = 110\Omega$, (Figure 11 and Figure 12)		30	50	ns
t_{SKEW}	Differential output delay skew			1	3	ns
$t_{ZH(SHDN)}$	Driver enable from shutdown to output high			30	50	ns
$t_{ZL(SHDN)}$	Driver enable from shutdown to output low			19	35	ns

Table 11. Receiver switching characteristics

$V_{CC} = 3V$ to $3.6V$, $T_A = -40$ to $85^\circ C$, unless otherwise specified. Typical values are referred to $T_a = 25^\circ C$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Propagation delay	$V_{ID} = 0V$ to $3V$, $C_{L1} = 15pF$ (Figure 13 and Figure 14)		30	50	ns
t_{RPDS}	$ t_{PLH} - t_{PHL} $ propagation delay skew	$V_{ID} = 0V$ to $3V$, $C_{L1} = 15pF$ (Figure 13 and Figure 14)		1	3	ns
t_{PZL}	Output enable time	$C_{RL} = 15pF$, (Figure 15 and Figure 19)		10	20	ns
t_{PZH}	Output enable time	$C_{RL} = 15pF$, (Figure 15 and Figure 19)		10	20	ns
t_{PHZ}	Output disable time	$C_{RL} = 15pF$, (Figure 15 and Figure 19)		10	20	ns
t_{PLZ}	Output disable time	$C_{RL} = 15pF$, (Figure 15 and Figure 19)		10	20	ns
$t_{ZH(SHDN)}$	Receiver enable from shutdown to output high	$C_{RL} = 15pF$, (Figure 15 and Figure 19)		10	20	ns
$t_{ZL(SHDN)}$	Receiver enable from shutdown to output low	$C_{RL} = 15pF$, (Figure 15 and Figure 19)		20	40	μs

- Note: 1 ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC} , respectively, when the DI input changes state.
- 2 Measured on $|t_{PLH}(A) - t_{PHL}(A)|$ and $|t_{PLH}(B) - t_{PHL}(B)|$
- 3 The transceivers are put into shutdown by bring RE high and DE low. If the input are in state for less than 80ns, the part are guaranteed not to enter shutdown. If the inputs are in this state for at least 300ns, the parts are guaranteed to have entered shutdown.

5 Test circuits and typical characteristics

Figure 3. Driver V_{OC} test load

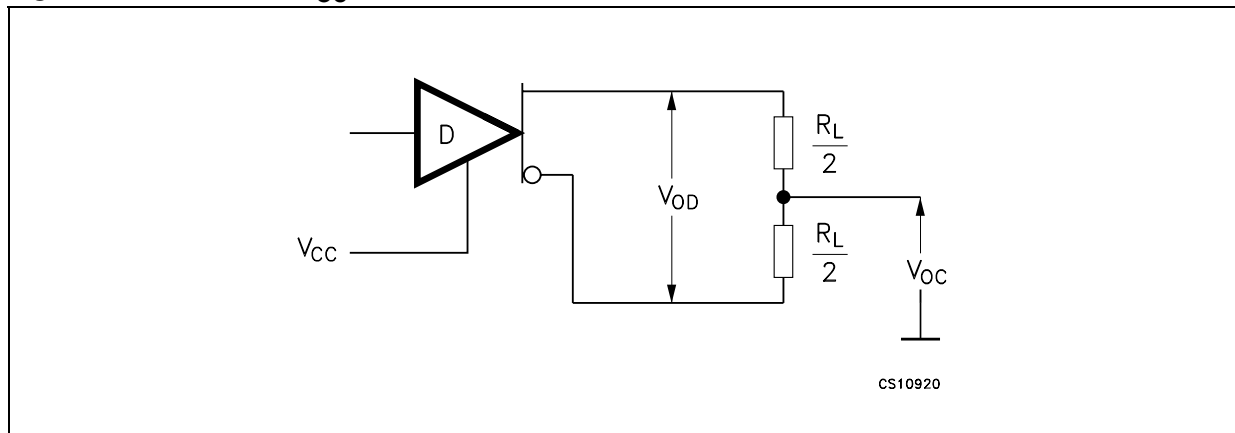


Figure 4. Driver V_{OD} with varying common mode voltage test load

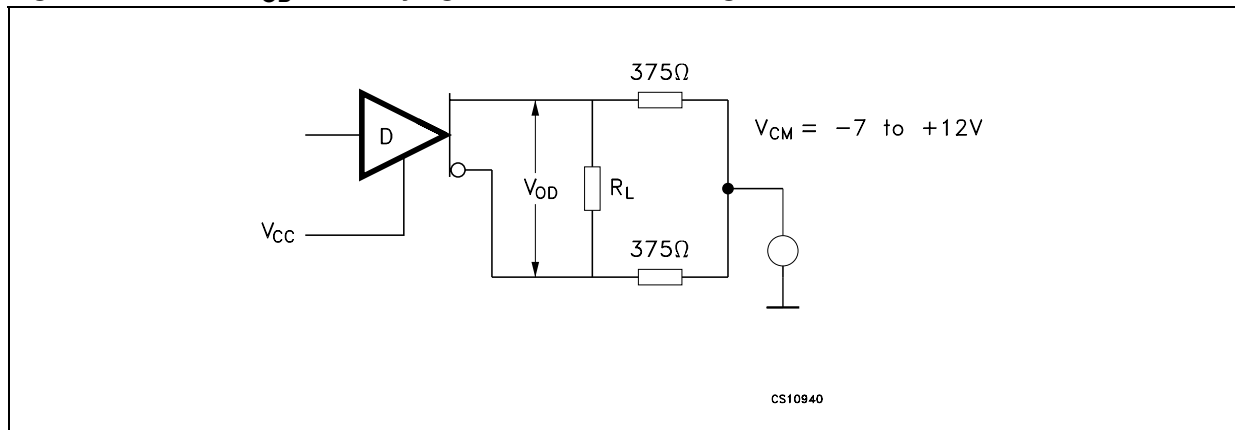


Figure 5. Receiver V_{OH} and V_{OL} test circuit

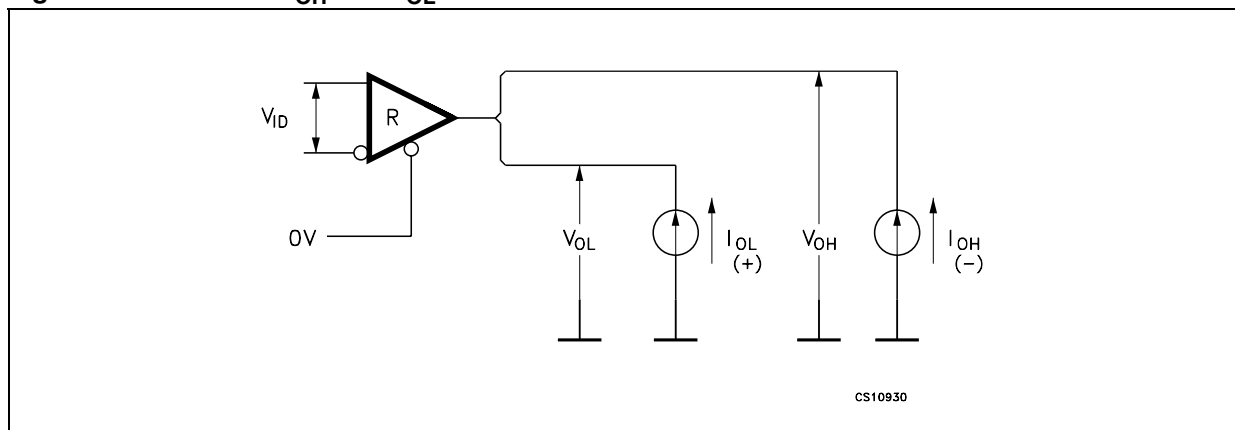


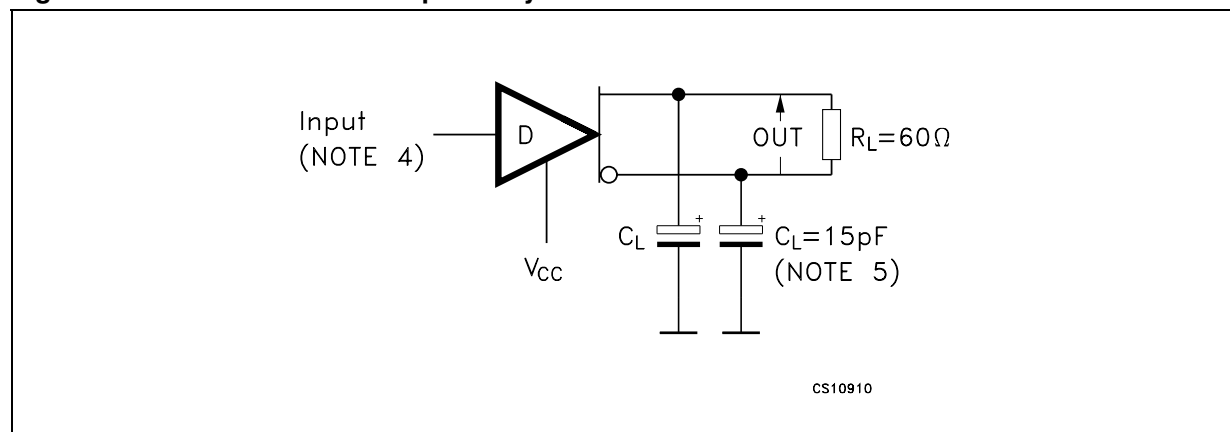
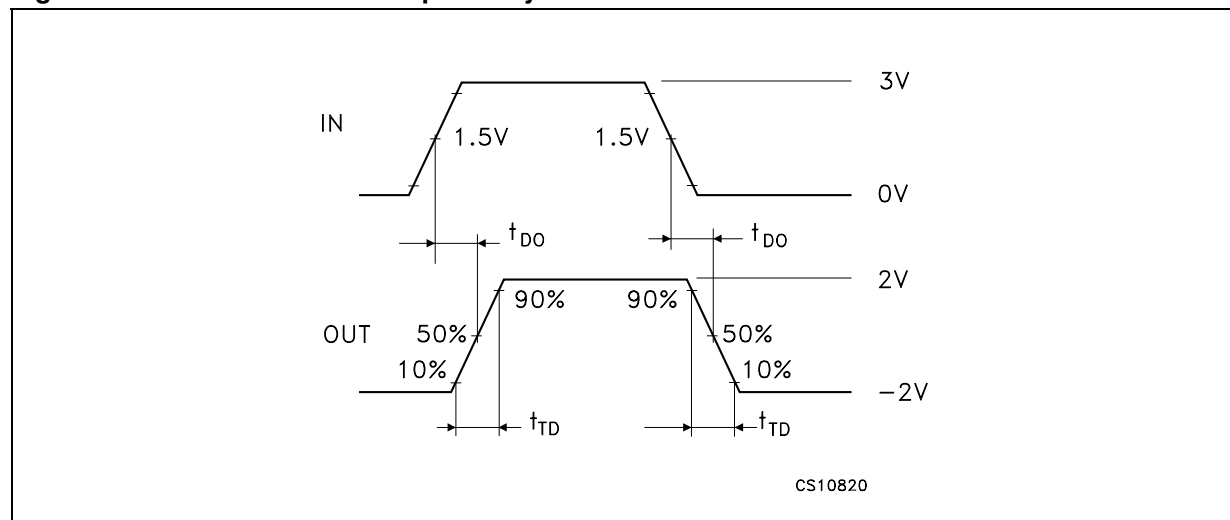
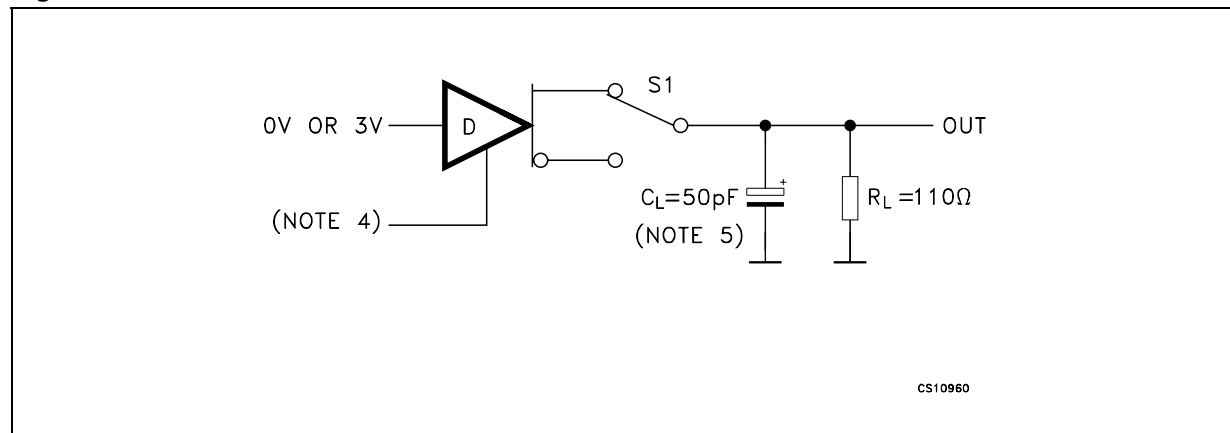
Figure 6. Drive differential output delay transition time test circuit**Figure 7. Drive differential output delay transition time waveform****Figure 8. Drive enable and disable times test circuit**

Figure 9. Drive enable and disable times waveforms

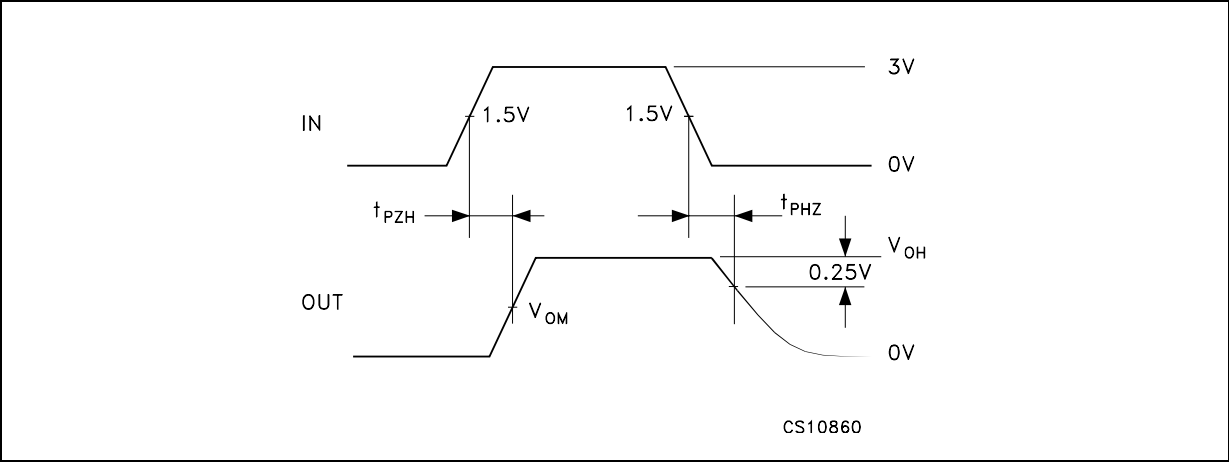


Figure 10. Drive propagation time test circuit

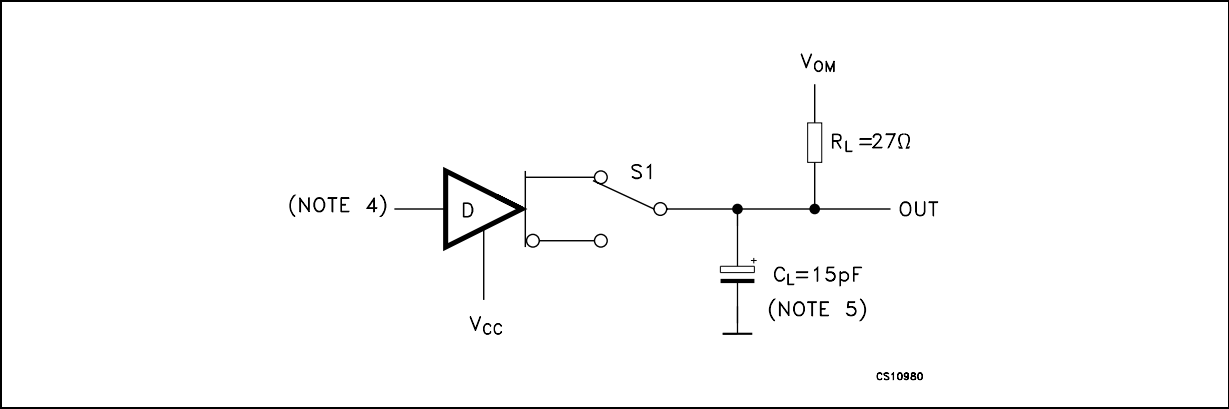


Figure 11. Drive propagation time waveform

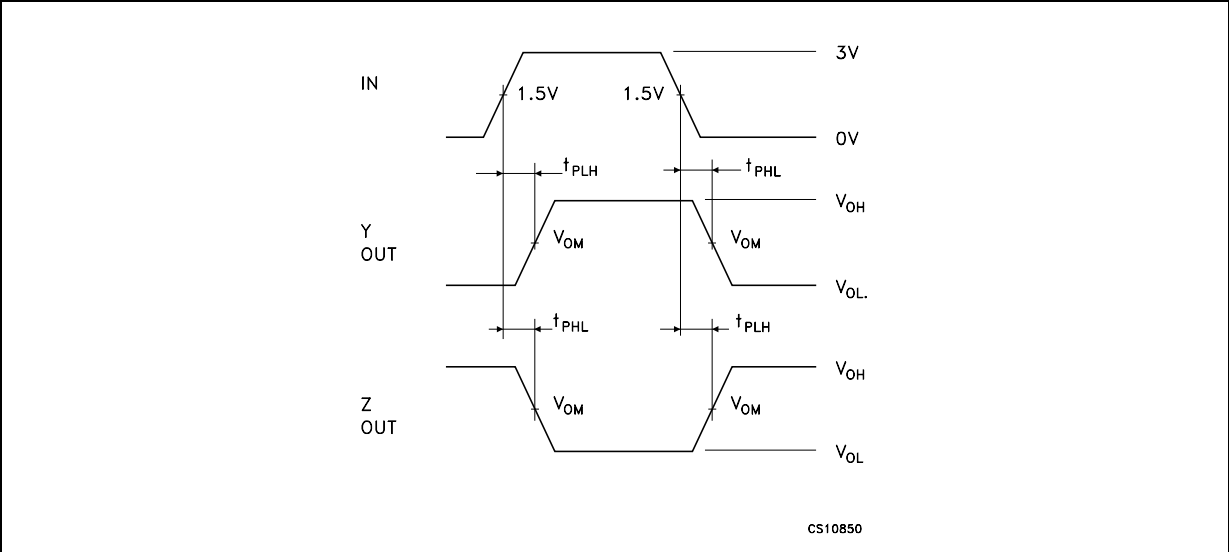


Figure 12. Drive enable and disable times test circuit

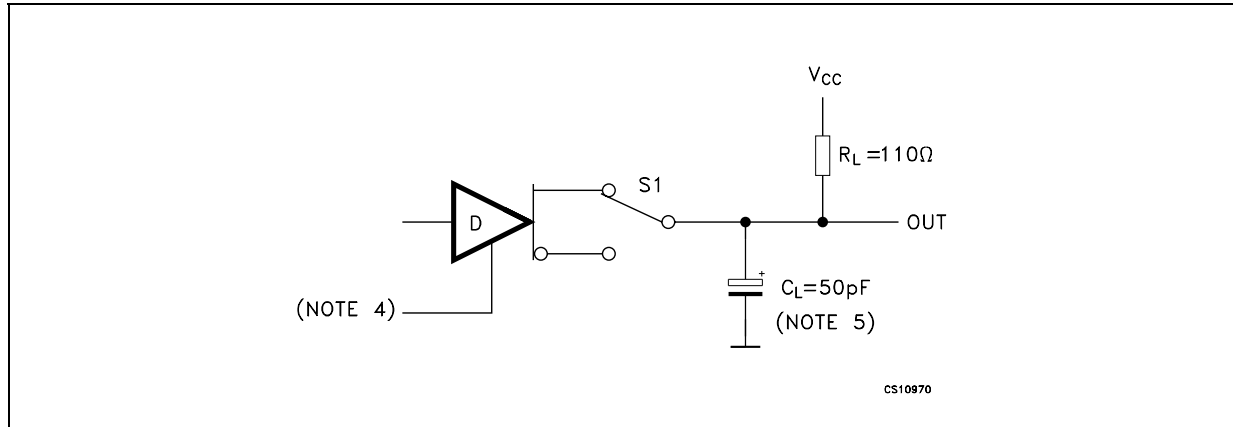


Figure 13. Drive enable and disable times waveforms

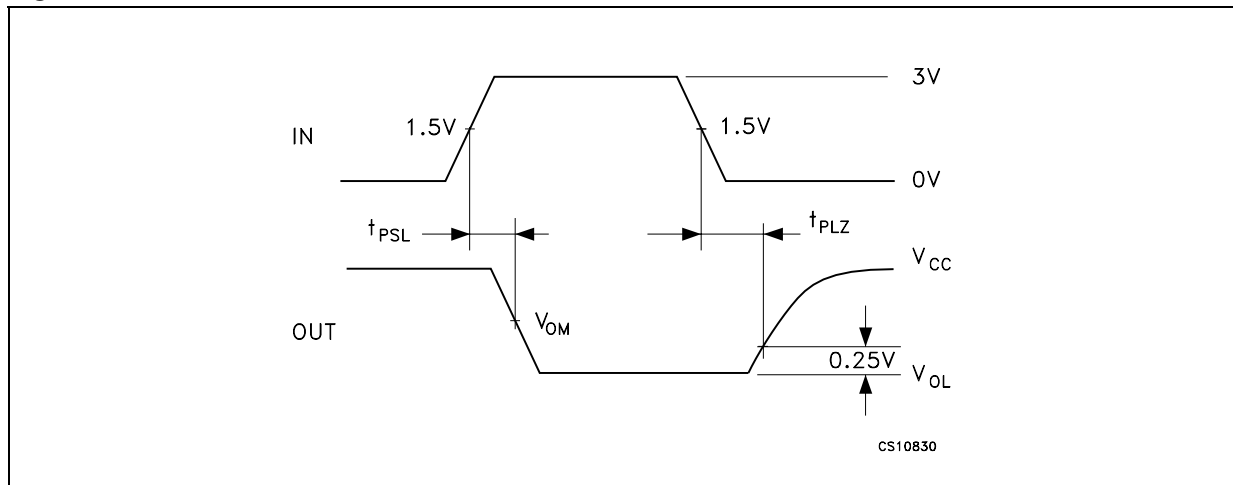
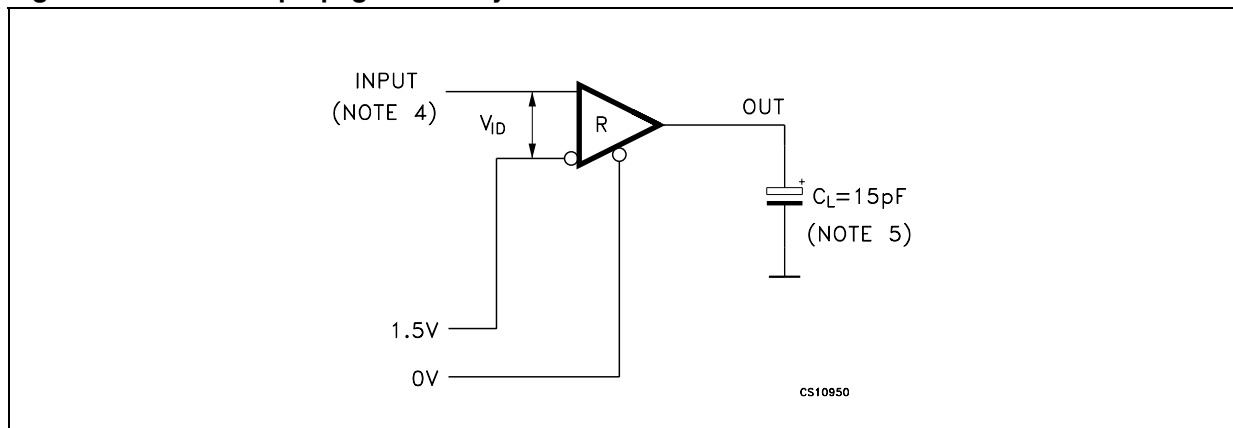


Figure 14. Receiver propagation delay time test circuit



Timing diagram for the CS10840 showing the relationship between the input (IN) and output (OUT) signals. The input signal (IN) is a trapezoidal pulse with a peak level of 3.0V and a low level of 0V. The output signal (OUT) is a trapezoidal pulse with a peak level of V_{CC} and a low level of 0V. The rising and falling edges of the input signal are labeled with 1.5V. The output signal is labeled with V_{OM} at its rising and falling edges. The propagation delay times t_{RPLH} and t_{RPHL} are indicated between the input and output signals.

Timing diagram for CS10870 showing IN and OUT signals. The diagram illustrates the relationship between the input (IN) and output (OUT) signals during a transition. The input signal (IN) transitions from a low level to a high level, then back to a low level. The output signal (OUT) transitions from a high level to a low level, then back to a high level. The output signal is shown with a delay relative to the input signal. Key voltage levels are 3V, 1.5V, and 0V. The output signal is labeled V_{OH} at the high level. The timing parameters t_{PRZH} and t_{PRSH} are indicated, representing the propagation delay from the input transition to the output transition. The diagram also shows the switch states: S1 OPEN, S2 CLOSED, and S3=1.5V.

Figure 18. Receiver enable and disable times waveform

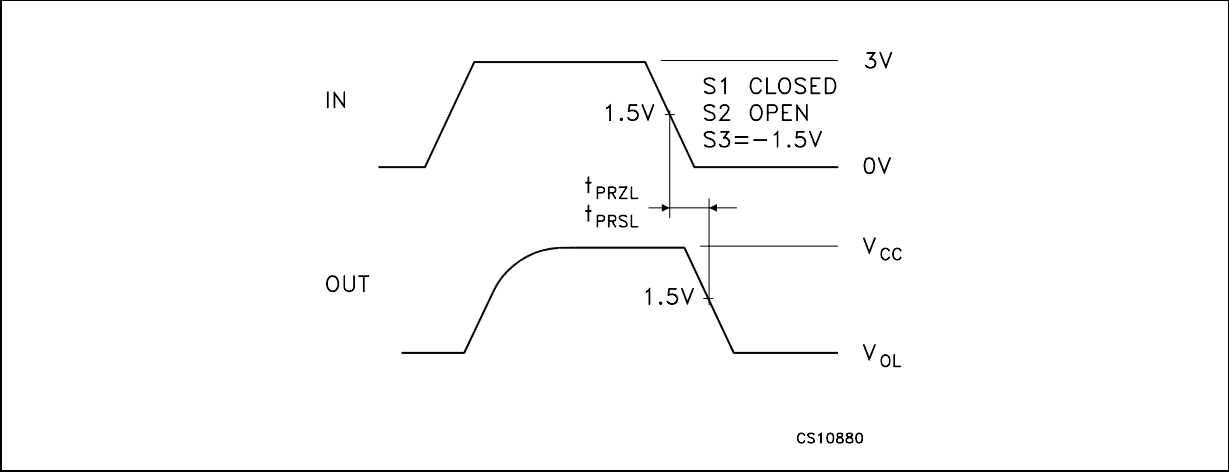


Figure 19. Receiver enable and disable times waveform

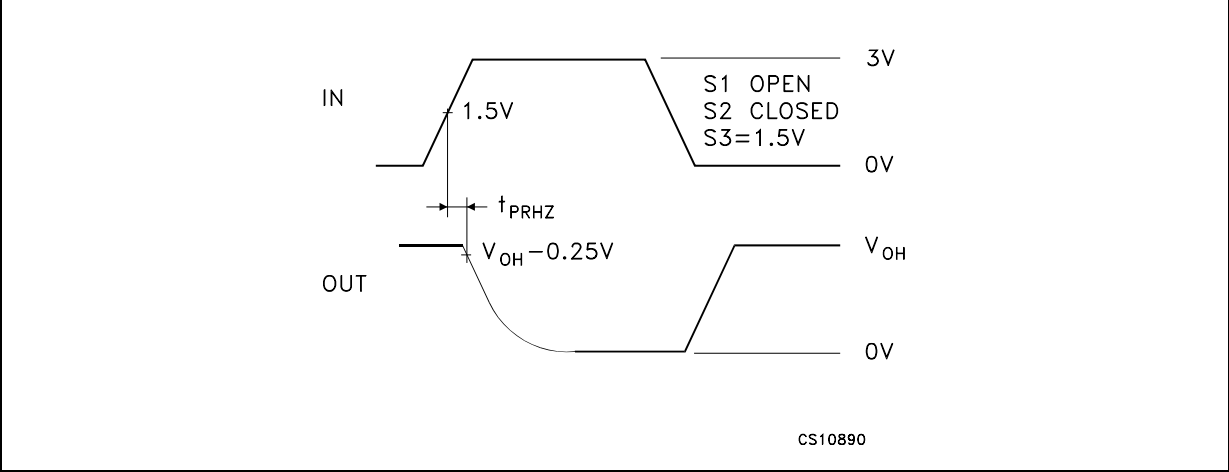


Figure 20. Receiver enable and disable times waveform

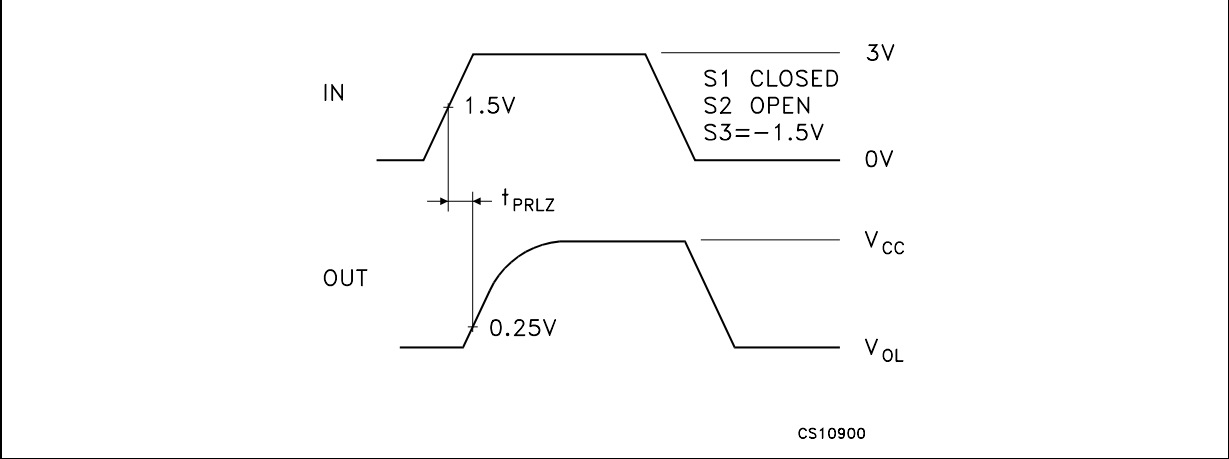


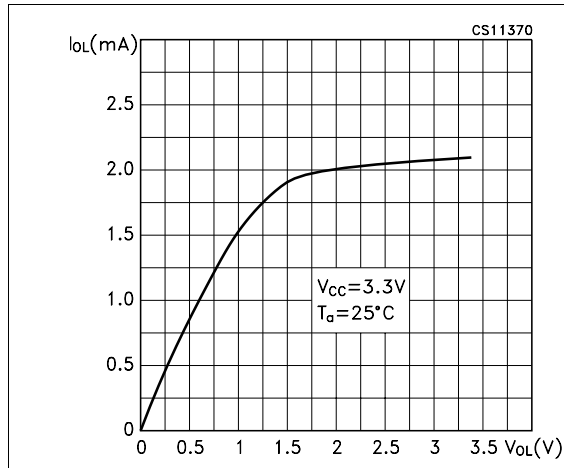
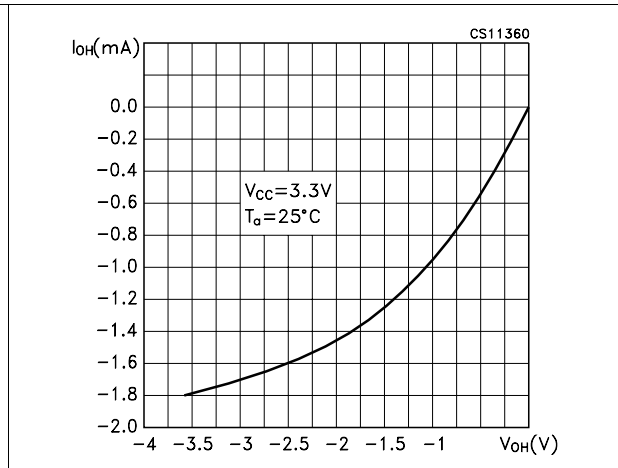
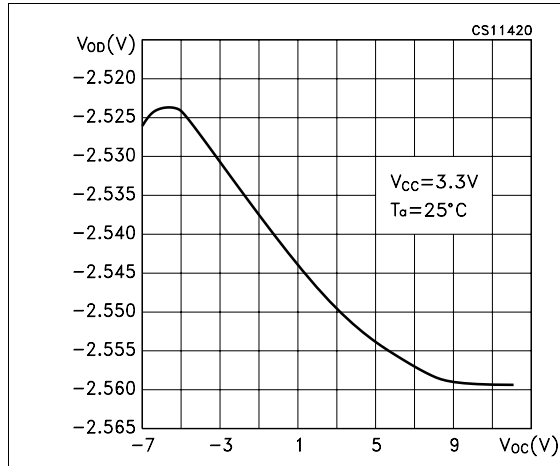
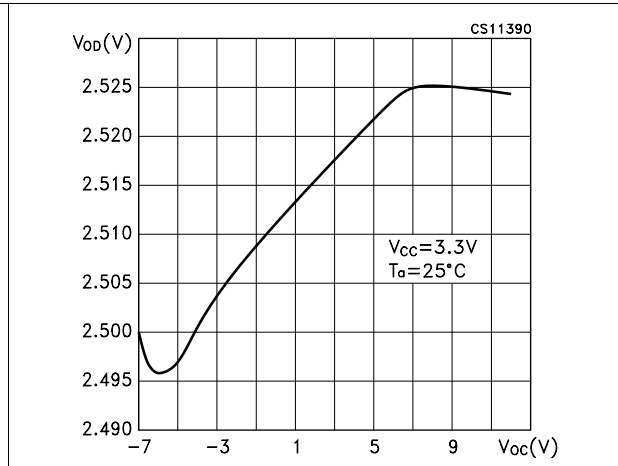
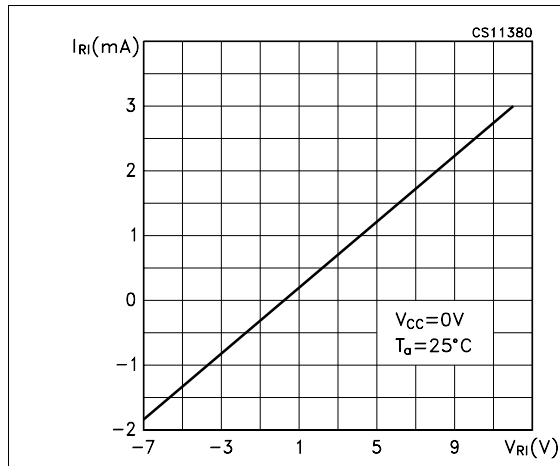
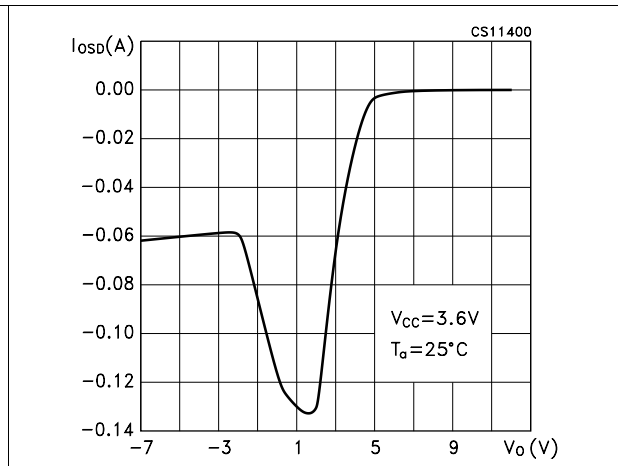
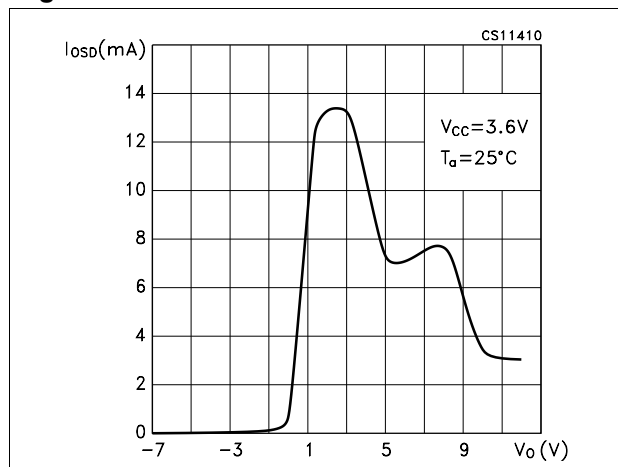
Figure 21. Receiver output current vs output low voltage**Figure 22. Receiver output current vs output high voltage****Figure 23. Low level driver output capability****Figure 24. High level driver output capability****Figure 25. Receiver input characteristics****Figure 26. Driver short circuit current**

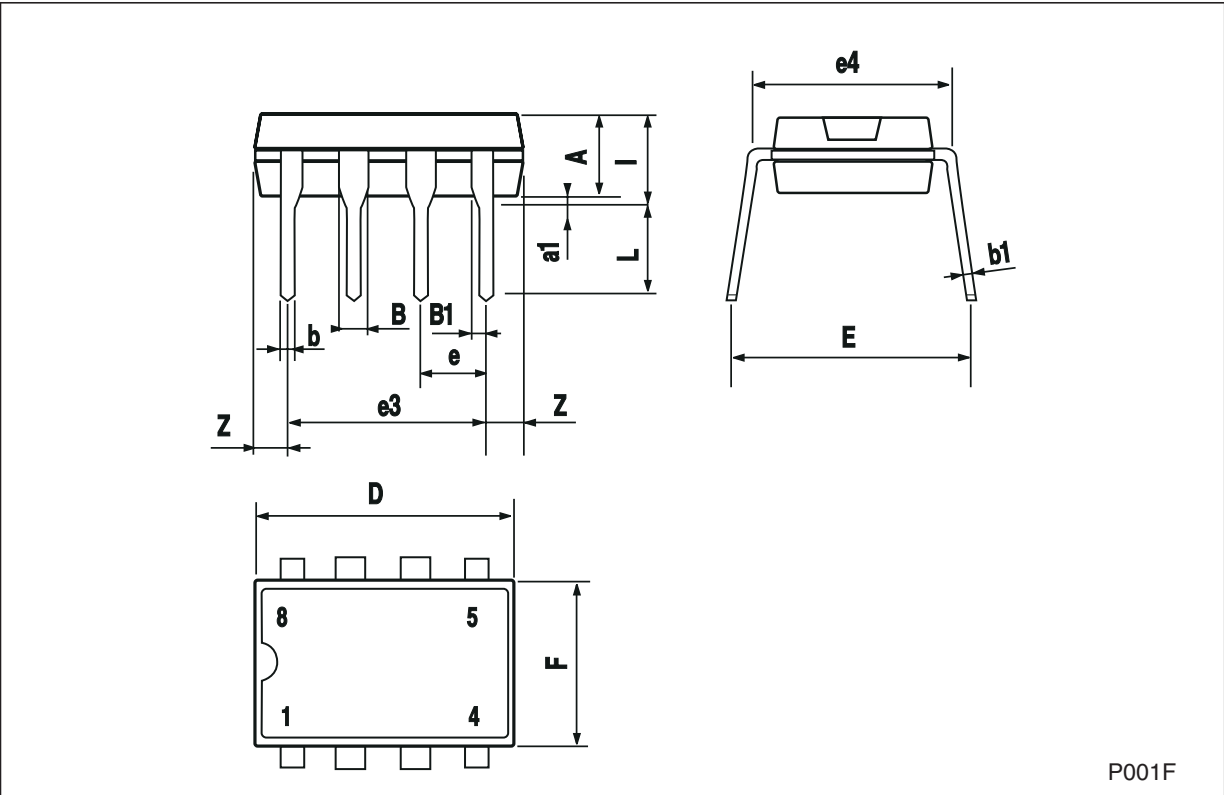
Figure 27. Driver short circuit current

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

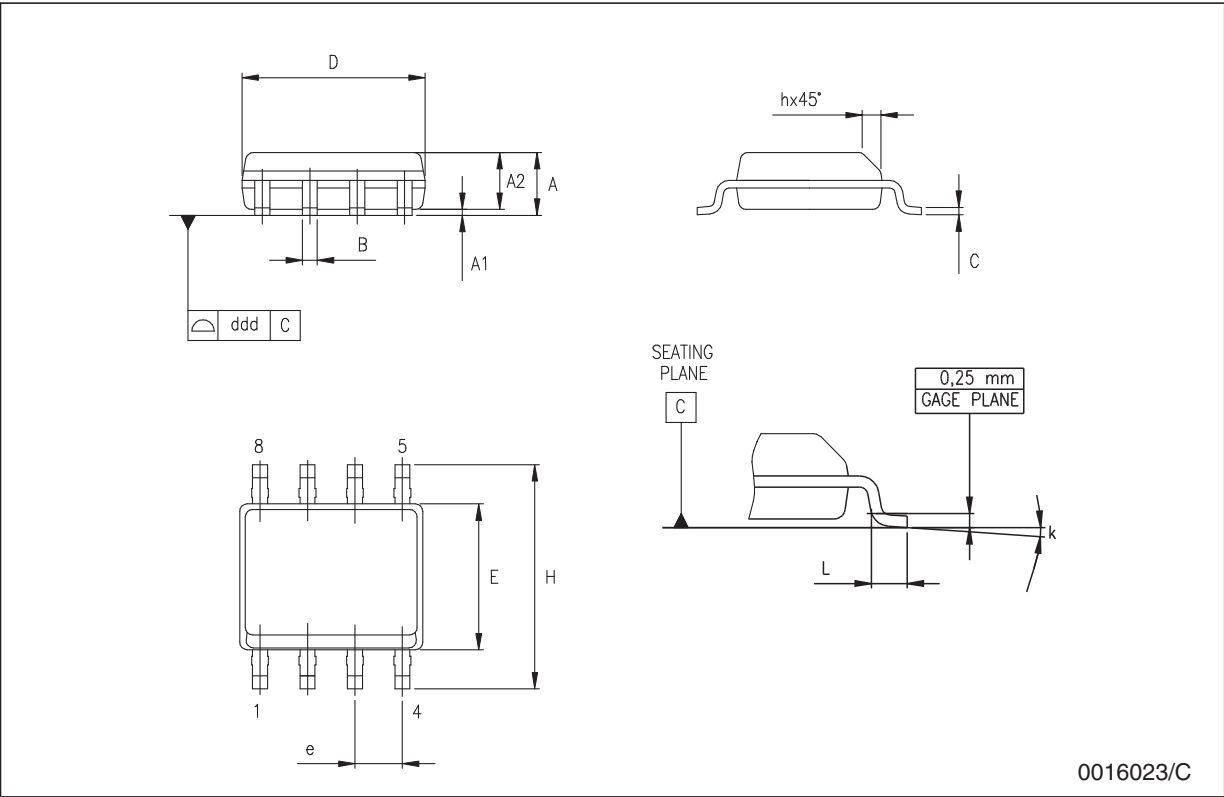
Plastic DIP-8 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063



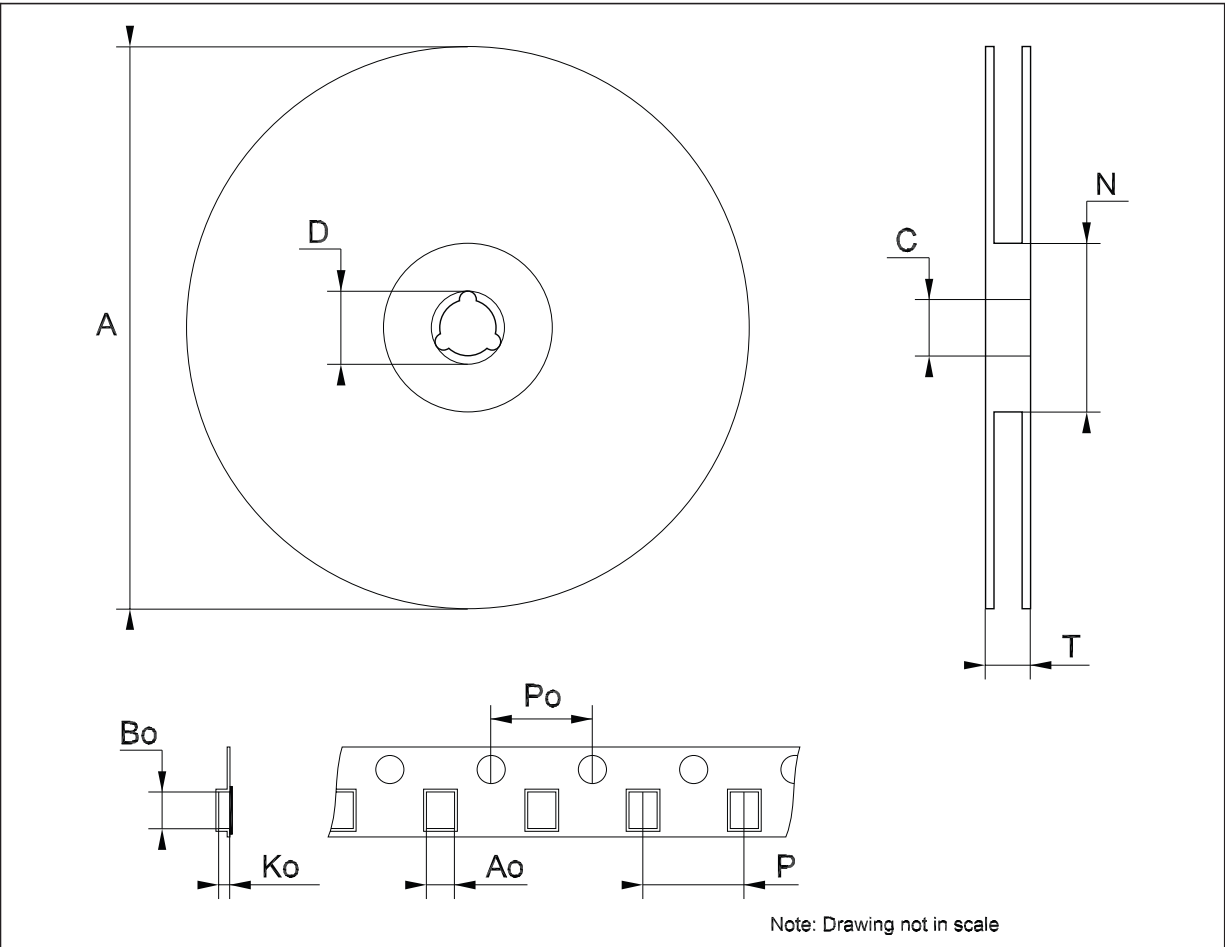
SO-8 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



Tape & reel SO-8 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	8.1		8.5	0.319		0.335
Bo	5.5		5.9	0.216		0.232
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



7 Revision history

Table 12. Document revision history

Date	Revision	Changes
02-May-2006	2	Order codes updated.
19-Nov-2007	3	Added Table 1 .

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